What is claimed is:

1. A serial bus data control device for being provided to communication equipment to receive two or more packets each being sent through a serial bus and each being composed of a header, actual data positioned subsequently to said header and a footer positioned subsequently to said actual data comprising:

a preprocessing section to recognize each of said two or more packets received through said serial bus and to divide at least said actual data contained in each of said recognized packets into two or more pieces of unit length data each having a predetermined data length; and

a storing section to temporarily store at least said actual data contained in each of said packets recognized by said preprocessing section;

whereby said preprocessing section is provided with an address control circuit to assign a continued address of said storing section, at least, to said unit length data constituting said actual data contained in each of said recognized packets composed of said header, said actual data and said footer.

2. The serial bus data control device according to claim 1, wherein said header contained in each of said packets has information about nodes on a sender side and on a receiver side and wherein a length of data of said header, said actual data and said footer is an integral multiple of a storing unit in said storing section.

3. The serial bus data control device according to claim 1, wherein said address control circuit performs addressing to store said header and said footer, in addition to addressing to store said actual data and is provided with

an address signal generating section to generate an address signal used to assign an address of said storing section to said header, said actual data and said footer, with an increment signal generating section to generate an increment signal used to sequentially add said address signal generated by said address signal generating section and to feed said generated increment signal to said address signal generating section and with a decrement signal generating section used to generate a decrement signal used to sequentially subtract said address signal to be generated by said address signal generating section and to feed said generated decrement signal to said address signal generating section and wherein, when an address is assigned to said header, a supply of said increment signal generated by said increment signal generating section and said decrement signal generated by said decrement signal generating section to said address signal generating section is stopped and, when an address is assigned to said unit length data constituting said actual data, said increment signal is fed from said increment signal generating section sequentially to add said address signal and, when an address is assigned to said footer, after said increment signal has been fed from said increment signal generating section to add said address signal for temporarily storing said footer in said storing section, said decrement signal generated by said decrement signal generating section is fed to said address signal generating section to subtract said address signal to be given to said footer for causing said footer to be overwritten by a header contained in a subsequently receiving packet.

4. The serial bus data control device according to claim 3, wherein said header is composed of two or more pieces of unit length data each having a unit length and wherein, when an address is assigned to each of said unit

length data contained in said header, by stopping a supply of said increment signal and said decrement signal to said address signal generating section to sequentially overwrite said unit length data contained in said header, the same address is assigned to said unit length data contained in said header.

5. The serial bus data control device according to claim 3, wherein, when an address is assigned to said unit length data contained in said actual data, a head address signal used to assign an address to unit length data placed in a head position in said two or more pieces of unit length data contained in said actual data matches an address signal for said header.

6. The serial bus data control device according to claim 3, wherein said footer is composed of two or more pieces of unit length data each having a unit length and wherein, after addressing has been performed by said address signal generating section to store each piece of said unit length data contained in said footer in said storing section, subtraction is done to match an address of said unit length data placed in a head position in said footer with that of a unit length data placed in a head position in a header contained in a subsequently receiving packet for causing said footer to be overwritten by said subsequent packet.

7. The serial bus data control device according to claim 1, wherein said storing section has a first data area to store said headers and footers contained in two or more packets in a manner so as to be arranged in a continuous state and a second data area to store two or more pieces of actual data contained in said two or more packets in a manner so as to be arranged in a continuous state.

8. The serial bus data control device according to claim 7, wherein each of said first data area and said second data area is composed of a single area.

9. The serial bus data control device according to claim 7, wherein said address control circuit performs addressing to store said header and said footer in addition to said addressing to store said actual data and is provided with a first address signal generating section to generate an address signal for assigning an address of said first data area to said header and said footer, with a second address signal generating section to generate an address signal for assigning an address of said second data area to said unit length data contained in said actual data, with an increment instruction signal generating section to generate a first increment instruction signal for sequentially adding said address signals produced by said first address signal generating section and a second increment instruction signal for sequentially adding said address signals produced by said second address signal generating section and to selectively feed said first and second increment instruction signals to said first and second address signal generating section and with a switching section to operate in accordance with said first and second increment instruction signals to feed selectively either of both said address signals produced by said first and second address generating sections to said storing section and wherein said increment instruction signal generating section, when an address is assigned to said header and said footer, sends out said first increment instruction signal to said first address generating section and, when an address is assigned to said actual data, sends out said second increment instruction signal to said second address generating section.

10. The serial bus data control device according to claim 9, wherein said

switching section connects said first and second address signal generating sections selectively to said storing section in accordance with said first increment instruction signal fed from said increment instruction signal generating section to feed said address signal to said storing section.

11. The serial bus data control section according to claim 9, wherein said increment instruction signal generating section is provided with a register to supply a signal expressing a value of said header, said actual data and said footer, with a first and second counters to count said value expressed by said signal fed from said register, with a first gate being operated in accordance with an output signal from each of said counters to send out said first increment instruction signal at the time of addressing to store said header and said footer and with a second gate being operated in accordance with an output signal from each of said counters to send out said second increment instruction signal at the time of addressing to store said actual data.

12. The serial bus data control device according to claim 11, wherein said second gate, when said first gate receives simultaneously a gate signal from said first counter and a gate signal from said second counter, receives simultaneously a first signal being complementary to said gate signal from said first counter and a second signal being complementary to said gate signal from said second counter.

13. The serial bus data control device according to claim 9, wherein each of said both areas in said storing section is partitioned to divided sections to correspond to each of said nodes so that each of packets received from two or more nodes through said serial bus is stored.

14. The serial bus data control device according to claim 13, each of said first and second data areas is composed of a single area.

15. The serial bus data control device according to claim 13, wherein said preprocessing section is provided with said address control circuits each corresponding to each of said nodes and with a node switching section to selectively supply an address signal fed from said address control circuits provided to correspond to each of said nodes to said storing section.

16. The serial bus data control section according to claim 15, wherein a storing capacity of each of said divided sections in said both data areas of said storing section is variable.

17. The serial bus data control section according to claim 16, wherein said storing capacity of each of said divided sections in said both data areas is able to be adjusted depending on a total amount of data of said header and said footer contained in each of two or more packets sent from each of said nodes and on a total amount of data of said actual data contained in each of two or more packets sent from each of said nodes.

18. The serial bus data control section according to claim 16, wherein each of said address control circuits corresponding to each of said nodes is provided with a first address register and a second address register to store an address showing a head portion of each of said divided sections and an address showing a tail portion of each of said divided sections for specifying each of said divided sections in each of said first and second data areas and wherein both said addresses assigned to said header and said footer to store in said

divided section are stored in said first address register and both said addresses assigned to said actual data to store in said divided section are stored in said second address register.